WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

forming a mesa structure from the semiconductor substrate, wherein the mesa structure has a first surface and first and second sidewalls;

forming a gate structure over the mesa structure, wherein the gate structure has a gate surface and first and second sides, and wherein first and second portions of the gate structure are disposed on the first and second sidewalls, respectively; and

doping portions of the semiconductor substrate adjacent the first and second sides of the gate structure.

2. The method of claim 1, wherein forming the gate structure includes forming a first layer of dielectric material over the mesa structure.

3. The method of claim 2, wherein forming the gate structure includes forming a second layer of dielectric material over the first layer of dielectric material.

4. The method of claim 2, wherein forming the first layer of dielectric material includes forming portions of the first layer of dielectric material over the first and second sidewalls, and wherein a portion of the first layer of dielectric material serves as the first portion of the gate structure and another portion of the first layer of dielectric material serves as the second portion of the gate structure.

5. The method of claim 4, wherein forming portions of the first layer of dielectric material over the first and second sidewalls includes oxidizing the first and second sidewalls.

6. The method of claim 2, further including forming a layer of semiconductor material over the semiconductor substrate adjacent the first and second sides of the gate structure.

7. The method of claim 6, wherein forming the layer of semiconductor material includes selectively growing the layer of semiconductor material.

8. The method of claim 7, wherein selectively growing includes selectively growing a semiconductor material selected from the group of semiconductor materials consisting of silicon, silicon germanium, and germanium.

9. The method of claim 7, wherein doping the semiconductor substrate comprises:

implanting a dopant into the layer of semiconductor material adjacent the first and second sides of the gate structure using an angled implant; and

implanting additional dopant into the layer of semiconductor material adjacent the first and second sides of the gate structure using a zero degree implant.

10. The method of claim 6, further including forming silicide from the layer of semiconductor material.

11. The method of claim 6, further including forming silicide from the gate structure.

12. The method of claim 11, wherein forming silicon from the layer of semiconductor material and from the gate structure includes forming nickel silicide.

13. The method of claim 1, wherein providing the semiconductor substrate includes providing a semiconductor-on-insulator semiconductor substrate.

14. A method for manufacturing a strained semiconductor device suitable for use in an integrated circuit, comprising:

providing a semiconductor-on-insulator mesa isolation structure, the semiconductor-on-insulator mesa isolation structure having a top surface and first and second sidewalls;

forming a gate dielectric material on the top surface and the first and second sidewalls;

forming a gate on the gate dielectric material, wherein the gate and the gate dielectric material cooperate to form a gate structure having a top surface and gate sidewalls;

forming a semiconductor material on portions of the top surface of the mesa isolation structure adjacent to the first and second sidewalls;

forming silicide from the semiconductor material; and

forming silicide from the gate, wherein the silicide from the gate strains the semiconductor device.

15. The method of claim 14, wherein providing the semiconductor-on-insulator mesa isolation structure includes forming portions of the first and second sidewalls to be below the top surface of the semiconductor-on-insulator mesa isolation structure.

16. The method of claim 14, wherein forming the gate dielectric material includes oxidizing the portions of first and second sidewalls below the top surface of the semiconductor-on-insulator structure.

17. The method of claim 14, wherein the forming the silicide from the gate includes forming nickel silicide.

18. The method of claim 14, wherein forming the semiconductor material on portions of the top surface of the mesa isolation structure includes forming a protective material over the gate before forming the semiconductor material.

19. A method for straining a semiconductor device, comprising:

providing a semiconductor substrate comprising a first layer of semiconductor material disposed over a layer of dielectric material, the semiconductor substrate having a top surface and isolation sidewalls;

forming a gate structure on the semiconductor substrate, the gate structure having a gate surface, first and second opposing gate sidewalls, and third and fourth opposing gate sidewalls; and

forming silicide from the gate surface and the first and second opposing gate sidewalls of the gate structure, wherein the silicide strains the semiconductor material of the semiconductor substrate.

20. The method of claim 19, further including forming a second layer of semiconductor material on the portions of the first layer of semiconductor material adjacent the third and fourth opposing gate sidewalls.

21. The method of claim 20, further including protecting the gate structure before forming the second layer of semiconductor material.

22. The method of claim 20, further including doping the second layer of semiconductor material.

23. The method of claim 22, further including forming silicide from the second layer of semiconductor material.

24. The method of claim 23, further including protecting the silicide formed from the second layer of dielectric material before forming the silicide from the gate surface.

25. A strained semiconductor device suitable for use in an integrated circuit, comprising:

a semiconductor-on-insulator substrate in a mesa isolation configuration;

a gate structure disposed on the semiconductor-on-insulator substrate, the gate structure having a gate surface, first and second opposing sidewalls, and third and fourth opposing sidewalls;

first and second doped regions adjacent the third and fourth opposing sidewalls, respectively, of the gate structure;

first and second silicide regions on the first and second doped regions, respectively; and

a gate silicide on the gate, wherein the gate silicide strains the semiconductor device.

26. The strained semiconductor device of claim 25, wherein the gate structure comprises a first dielectric material disposed on a second dielectric material and a semiconductor material disposed on the first dielectric material.

27. The strained semiconductor device of claim 26, wherein the first dielectric material is oxide, the second dielectric material is silicon nitride, and the semiconductor material is polysilicon.

28. The strained semiconductor device of claim 26, wherein the gate dielectric material further includes sidewall oxide disposed on the first and second opposing sidewalls.

29. The strained semiconductor device of claim 25, wherein the silicide on the gate and the first and second silicide regions comprises silicide selected from the group of silicides consisting of nickel silicide, tin silicide, titanium silicide, and cobalt silicide.